Fibocom
PERFECT WIRELESS EXPERIENCE

FG132-M.2-10 Hardware Guide

V1.1

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Contents

Applicable Models

No.	Applicability Model	Description
1	FG132-GL-00-M2-10	5G Redcap, 2Gb FLASH, 2Gb DDR, GL Band, Main ANT, Div ANT, GNSS ANT, 4G/5G, 3042 package

Change History

V1.1 (2025-2-25)	Modify SRS description
V1.0 (2025-1-6)	Initial version

1 Foreword

1.1 Description

By reading this document, you can quickly understand the interface specifications, electrical characteristics, mechanical dimensions and other special requirements information of the module. With the User Manual provided by Fibocom, you can quickly perform circuit design and debugging of the wireless part.

1.2 Reference Standards

This product is designed with reference to the following standards:

- 3GPP TS 36.521-1 V15.0.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- 3GPP TS 38.300 V15.5.0 : 3rd Generation Partnership Project; Technical Specification Group Radio Access Network; NR; NR and NG-RAN Overall Description; Stage 2
- 3GPP TS 38.521-1 V15.2.0 : User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Range 1 Standalone;
- 3GPP TS 38.521-3 V15.2.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 3: Range 1 and Range 2 Interworking operation with other radios;
- 3GPP TS 36.124V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit (USAT)
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPPTS27.005 V10.0.1: Use of Data Terminal Equipment -Data Circuit terminating Equipment (DTE – DCE)interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
- PCI_Express_M.2_Specification_Rev1.1_TS_12092016_NCB
- Universal Serial Bus Specification 2.0

2 Product Overview

2.1 General Description

FG132-M.2 series module is a highly integrated 5G wireless communication module, which adopts standard M.2 Key-B interface and supports LTE-FDD/LTE-TDD/5G-NR network systems. The module can provide stable and high-speed data transmission services, suitable for most mobile carrier's networks in the world.

Table 1. Operating bands

Model	Antenna Quantity	Band	Band Configuration
FG132-GL-00	3	5G NR	SA: n1/2/3/5/7/8/12/13/14/18/20/25/26/28/30/38/40/41/48/66/70/71/77/78
		LTE	LTE: B1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/30/34/38/39/40/41/42/43/48/66/71
		GNSS	GPS/GLONASS/BDS/Galileo/QZSS

2.2 Key Features

Table 2. Key features

Category	Function Description
Power supply	DC: 3.135~4.4V; typical value: 3.8V
Operating system of host computer	Linux / Android / Windows
Network protocol	IPv4/IPv6
SMS	Supported
Memory	2Gb DDR2 + 2Gb NAND Flash
Function interface	Dual SIM cards: support 3 V/1.8 V and SIM hot plug function
	USB×1: USB2.0, Used for AT command communication, data transmission, software debugging and firmware upgrade
	PCM×1: Used for audio function with external codec; Support 16-bit linear data format; Support long frame synchronization and short frame synchronization; Support master and slave modes
	PCIe×1: Compliant with PCIe Gen 2, 1 lane; Support RC and EP mode
	ANT_CTL x4

Category	Function Description
	ANT x3: Main ANT, Div ANT, GNSS ANT
LTE features	UL supports QPSK, 16QAM and 64QAM modulations DL supports QPSK, 16QAM, 64QAM and 256QAM modulations LTE: A maximum uplink rate of 75Mbps and a maximum downlink rate of 195Mbps
5G NR features	UL supports QPSK, 16QAM, 64QAM, 256QAM and PI/2 BPSK modulations DL supports QPSK, 16QAM, 64QAM and 256QAM modulations A maximum uplink rate of 123 Mbps and a maximum downlink rate of 223 Mbps
RF Power level	5G NR Band: Class 3 (23 dBm ±2 dB) LTE Band: Class 3 (23 dBm ±2 dB) LTE HPUE Band: Class 2 (26 dBm ±2 dB) FG132-GL-00: B38/40/41/42/43
5G SRS	Support 1T2R FG132-GL-00: n38/40/41/48/77/78
GNSS features	Supports dual-band GNSS: L1/L5 Supports GPS, GLONASS, BDS, Galileo/ QZSS Supports Gen 9 v5.1 engine Protocol: NMEA 0183 Data update rate: 1 Hz by default
Physical characteristics	Dimensions: (42.0±0.15) mm x (30.0±0.15) mm x (3.2±0.3) mm Encapsulation: M.2 Weight: about 8g
Temperature characteristics	Operating temperature: -35°C~+75°C. The module can work normally and meet the requirements of 3GPP standard. Extended temperature: -40°C~+85°C. The module can work normally, and some performance indicators may exceed the requirements of 3GPP standard. Storage temperature: -45°C~+90°C, normal storage temperature range when the module is not powered on.
Upgrade Software	By USB/FOTA
Environmental protection standard	RoHS, HF

2.3 Hardware Block Diagram

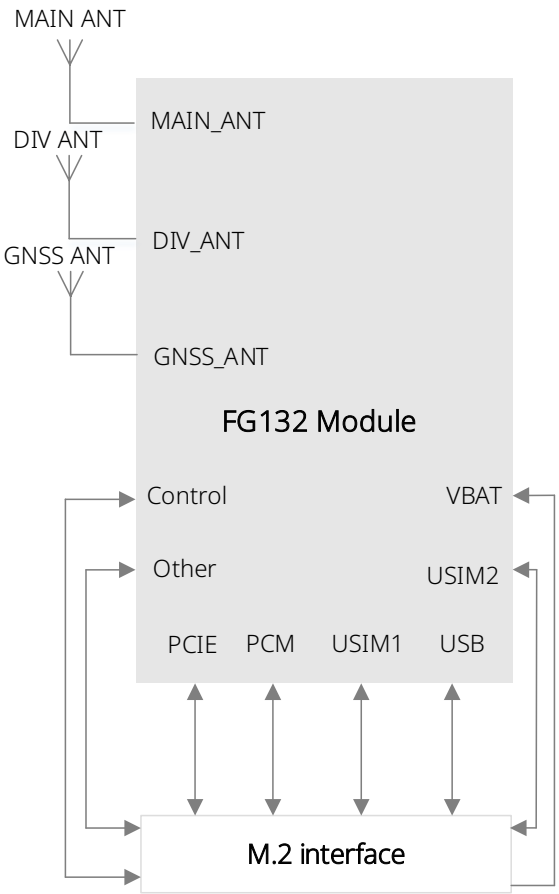

Figure 1. Hardware block diagram

The above figure is the hardware block diagram of the module, which mainly introduces the key components and functions of the baseband and radio frequency parts.

- M.2 Interface: module interface.
- FG132 Module
- MAIN ANT
- DIV ANT
- GNSS ANT

2.4 Description of Development kit

Fibocom configures a complete development kit for the module, which is convenient for users to quickly understand the performance of the module. For details about development board usage, see *Fibocom_EVB-M2-F01_User Guide*.

3 Pin Definition

3.1 Pin Distribution

74	VBAT	NC	75
72	VBAT	GND	73
70	VBAT	GND	71
68	NC	GND	69
66	SIM1_DET	RESET#	67
64	COEX_TXD	VDD_EXT	65
62	COEX_RXD	GNSS_PPS *	63
60	COEX3	GRFC2	61
58	RFFE_DATA	GRFC1	59
56	RFFE_CLK	GND	57
54	PEWAKE#	REFCLKp	55
52	CLKREQ#	REFCLKn	53
50	PERST#	GND	51
48	SIM2_PWR	PERp0	49
46	SIM2_RST	PERn0	47
44	SIM2_CLK	GND	45
42	SIM2_DATA	PETp0	43
40	SIM2_DET	PETn0	41
38	WAKEUP_IN	GND	39
36	SIM1_PWR	NC	37
34	SIM1_DATA	NC	35
32	SIM1_CLK	GND	33
30	SIM1_RST	NC	31
28	PCM_SYNC	NC	29
26	W_DISABLE2# *	GND	27
24	PCM_OUT	DPR *	25
22	PCM_IN	WAKEUP_OUT	23
20	PCM_CLK	NC	21
	Notch	Notch	
	Notch	Notch	
	Notch	Notch	
	Notch	Notch	
10	LED1#	GND	11
8	W_DISABLE1#	USB D-	9
6	FULL_CARD_POWER_OFF#	USB D+	7
4	VBAT	GND	5
2	VBAT	GND	3
		NC	1

Figure 2. Pin distribution

3.2 Pin Description

Table 3. I/O type parameter definition

Type	Description	Type	Description
PI	Power input	AIO	Analog input and output
PO	Power output	OD	Open drain
DI	Digital input	PU	High level by pulling up
DO	Digital output	PD	Low level by pulling down
DIO	Digital input and output	T	Tristate, namely, high resistance, determined by the peripheral circuit
AI	Analog input	G	Ground
AO	Analog output	Unstable	The voltage level is unstable, and the software is uncontrollable for a period of time after power on. The waveform is unstable, and it is not recommended to connect devices that are sensitive to the voltage level

Table 4. Pin description

Pin No.	Pin Name	I/O	Reset Value[1]	Pin Description	DC Characteristics
1	NC	- -	- -	- -	- -
2	VBAT	PI	- -	M.2 Power supply	3.135~4.4V
3	GND	- -	- -	Ground	- -
4	VBAT	PI	- -	M.2 Power supply	3.135~4.4V
5	GND	- -	- -	Ground	- -
6	FULL_CARD_POWER_OFF#	DI	- -	Module power on control, high-level startup	3.3V/1.8V
7	USB D+	AIO	- -	USB 2.0 data +	- -
8	W_DISABLE1#	DI	PD	Flight mode control 1, external control module enters flight mode, active low	3.3V/1.8V
9	USB D-	AIO	- -	USB 2.0 data -	- -
10	LED1#	OD	- -	RF status indication	- -
11	GND	- -	- -	Ground	- -
12	Notch	- -	- -	Notch	- -
13	Notch	- -	- -	Notch	- -

Pin No.	Pin Name	I/O	Reset Value[1]	Pin Description	DC Characteristics
14	Notch	- -	- -	Notch	- -
15	Notch	- -	- -	Notch	- -
16	Notch	- -	- -	Notch	- -
17	Notch	- -	- -	Notch	- -
18	Notch	- -	- -	Notch	- -
19	Notch	- -	- -	Notch	- -
20	PCM_CLK	DO	PD	PCM clock	1.8V
21	NC	- -	- -	- -	- -
22	PCM_IN	DI	PD	PCM data receive	1.8V
23	WAKEUP_OUT	DO	PD	Wakeup host	1.8V
24	PCM_OUT	DO	PD	PCM data transmission	1.8V
25	DPR *	DI	- -	Dynamic power control, used for SAR interrupt detection, effective at low levels	3.3V/1.8V
26	W_DISABLE2# *	DI	- -	Flight mode control 2, active low, reserved	3.3V/1.8V
27	GND	- -	- -	Ground	- -
28	PCM_SYNC	DO	PD	PCM synchronization	1.8V
29	NC	- -	- -	- -	- -
30	SIM1_RST	DO	Unstable	SIM1 card reset	3V/1.8V
31	NC	- -	- -	- -	- -
32	SIM1_CLK	DO	PD	SIM1 card clock	3V/1.8V
33	GND	- -	- -	Ground	- -
34	SIM1_DATA	DIO	PD	SIM1 card data, pull up internal	3V/1.8V
35	NC	- -	- -	- -	- -
36	SIM1_PWR	PO	- -	SIM1 card power	3V/1.8V
37	NC	- -	- -	- -	- -
38	WAKEUP_IN	DI	PD	External wake-up module	1.8V
39	GND	- -	- -	Ground	- -
40	SIM2_DET	DI	PD	SIM2 card hot plug	1.8V
41	PETn0	AO	- -	Negative end of PCIe data sending	- -

Pin No.	Pin Name	I/O	Reset Value[1]	Pin Description	DC Characteristics
42	SIM2_DATA	DIO	PD	SIM2 card data, pull up internal	3V/1.8V
43	PETp0	AO	- -	Positive end of PCIe data sending	- -
44	SIM2_CLK	DO	PD	SIM2 card clock	3V/1.8V
45	GND	- -	- -	Ground	- -
46	SIM2_RST	DO	PD	SIM2 card reset	3V/1.8V
47	PERn0	AI	- -	Negative end of PCIe data receiving	- -
48	SIM2_PWR	PO	- -	SIM2 card power	3V/1.8V
49	PERp0	AI	- -	Positive end of PCIe data receiving	- -
50	PERST#	DIO	PD	PCIe reset	3.3V/1.8V
51	GND	- -	- -	Ground	- -
52	CLKREQ#	DIO	Unstable	PCIe clock request	3.3V/1.8V
53	REFCLKn	AIO	- -	PCIe reference clock Difference negative end	- -
54	PEWAKE#	DIO	Unstable	PCIe wakeup	3.3V/1.8V
55	REFCLKp	AIO	- -	PCIe Reference Clock Difference positive end	- -
56	RFFE_CLK	DO	PD	RFFE-MIPI serial clock signal	1.8V
57	GND	- -	- -	Ground	- -
58	RFFE_DATA	DIO	PD	RFFE-MIPI serial data signal	1.8V
59	GRFC1	DO	PD	General GPIO of RF 1	1.8V
60	COEX3	DI	PD	5G/LTE and WLAN COEX interface	1.8V
61	GRFC2	DO	PD	General GPIO of RF 2	1.8V
62	COEX_RXD	DI	PD	5G/LTE and WLAN COEX UART receiving	1.8V
63	GNSS_PPS *	DO	- -	GNSS Timing	1.8V
64	COEX_TXD	DO	PD	5G/LTE and WLAN COEX UART sending	1.8V
65	VDD_EXT	PO	- -	Digital IO power supply	1.8V
66	SIM1_DET	DI	PD	SIM1 card hot plug	1.8V
67	RESET#	DI	- -	M.2 reset, active low	1.8V/3.3V

Pin No.	Pin Name	I/O	Reset Value[1]	Pin Description	DC Characteristics
68	NC	- -	- -	- -	- -
69	GND	- -	- -	Ground	- -
70	VBAT	PI	- -	M.2 Power supply	3.135~4.4V
71	GND	- -	- -	Ground	- -
72	VBAT	PI	- -	M.2 Power supply	3.135~4.4V
73	GND	- -	- -	Ground	- -
74	VBAT	PI	- -	M.2 Power supply	3.135~4.4V
75	NC	- -	- -	- -	- -

- Reset Value: Status of the pin during initialization.
- "*" indicates a reserved function, which has not been developed. If you need to use such a function, consult and communicate with Fibocom FAE.

4 Application Interfaces

4.1 Power Interface

Table 5. VBAT parameter

Parameter		Min	Typical	Max	Unit
Electrical feature	VBAT	3.135	3.8	4.4	V
Absolute Maximum		-0.3	- -	4.7	V

To reduce voltage drop, two filter capacitors of 100 μF with low ESR (ESR≤0.7Ω) are required. It is also recommended to reserve 5 chip multilayer ceramic capacitors (MLCC) with good ESR performance (22μF, 100nF, 6.8nF, 220pF, and 68pF) for VBAT(Pin2/4) and 7 chip multilayer ceramic capacitors (MLCC) with good ESR performance (22μF, 100nF, 220pF, 68pF, 15pF, 9.1pF, and 4.7pF) for VBAT(Pin70/72/74), and the capacitors should be placed close to the VBAT pin. A star topology is required for VBAT when an external power supply is connected to the module. The VBAT trace width is not less than 2.6mm. According to design rules, the longer the VBAT trace, the wider the trace width.

In addition, to suppress power fluctuations and shocks and ensure the stability of the output power supply, it is recommended to add a TVS array with a reverse operating voltage of 4.5V, low clamp voltage and high reverse pulse current at the front end of the power supply. The recommended model is ESDH4V5P1. The power star topology is shown in the following figure.

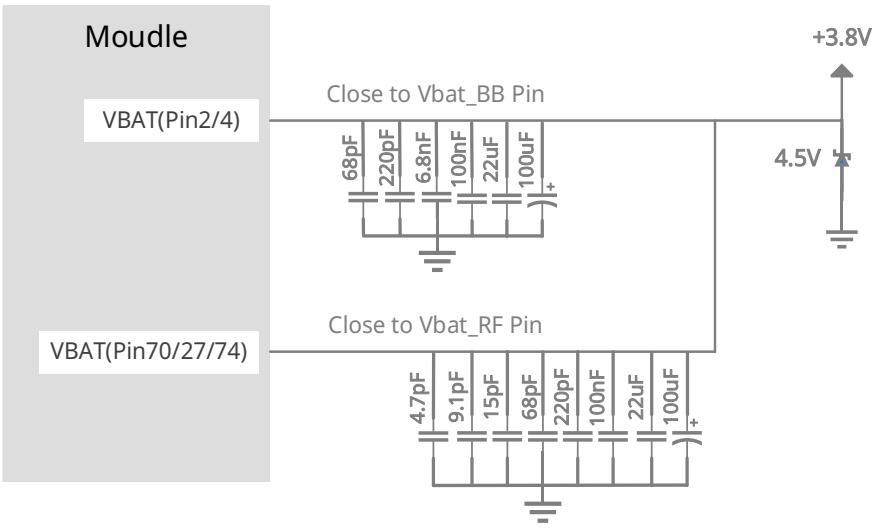

Figure 3. Reference circuit of power supply

The filter capacitor should be placed close to the power pin. The smaller the capacitance, the closer it is to the corresponding power pin. The filter capacitor is placed on the same side as the module. Ensure that it is not in a different layer. Otherwise, there will be a risk of TIS interference, and the wiring should be as short and wide as possible.

- The customer can adjust the recommended filter capacitor according to the actual situation, and the value is not fixed.
- It is recommended to increase the power supply control circuit of the module, the power supply of the module is controlled by the host computer, and when the module cannot be reset normally, the host computer can be used to control the module to power off and power on again, which can avoid the problem that the module cannot be reset after the software hang.

The customer should choose a DC chip with a continuous output capability of greater than 2.6 A. The recommended input voltage of the module is 3.8 V, and the ripple should be less than 150 mV. Add a voltage stabilizing capacitor to ensure that the VBAT voltage will not continue to be lower than 3.135 V for more than 2 ms during the operating of the module. Otherwise, the module will trigger the shutdown mechanism. The following figure shows the power supply requirements.

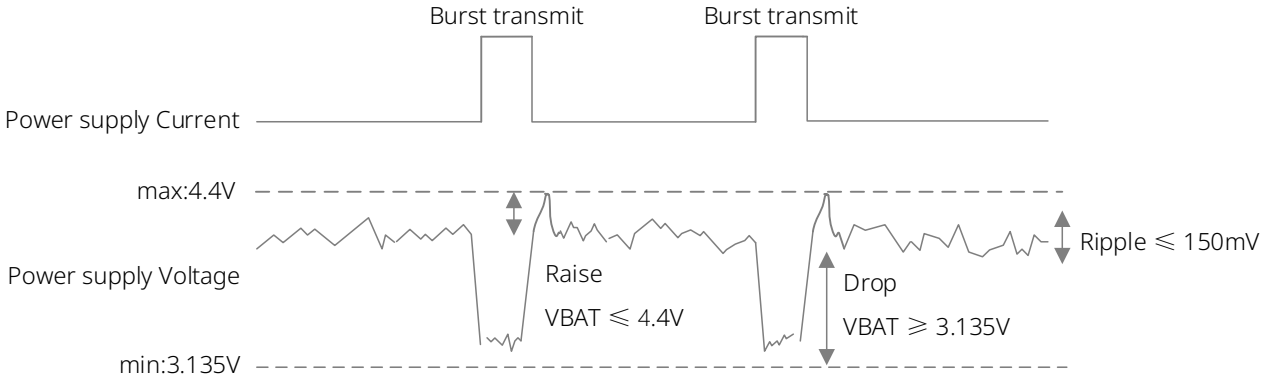

Figure 4. Power supply requirements

Due to the large peak current (about 2.6A) when the 5G module is operating, the VBAT voltage fluctuation will gradually decrease with the increase of the voltage stabilizing capacitor. However, it is impossible to eliminate the VBAT voltage fluctuation. Therefore, the power system of the module must be separated from the power supply of other main control chips to avoid voltage fluctuations affecting the power stability of the main control chip and causing the system to shut down.

4.2 FCPO# Interface

When the module is in the power-off state, it can be powered on by pulling up the FCPO# pin for 0.1s to 2s. It is recommended to use host GPIO circuit to control FCPO#. The power on/off circuit is shown in the following figure.

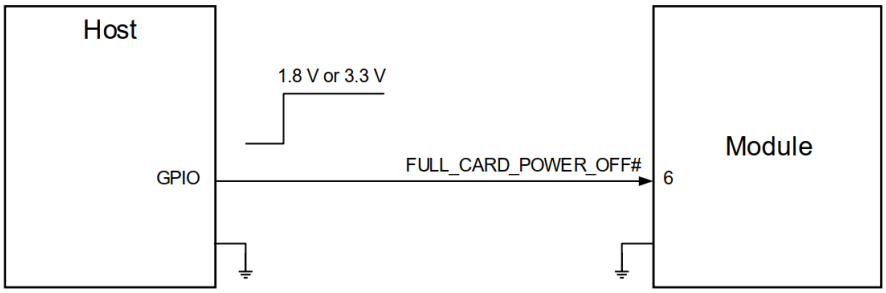

Figure 5. Power on/off circuit

The module power-on process is as follows:

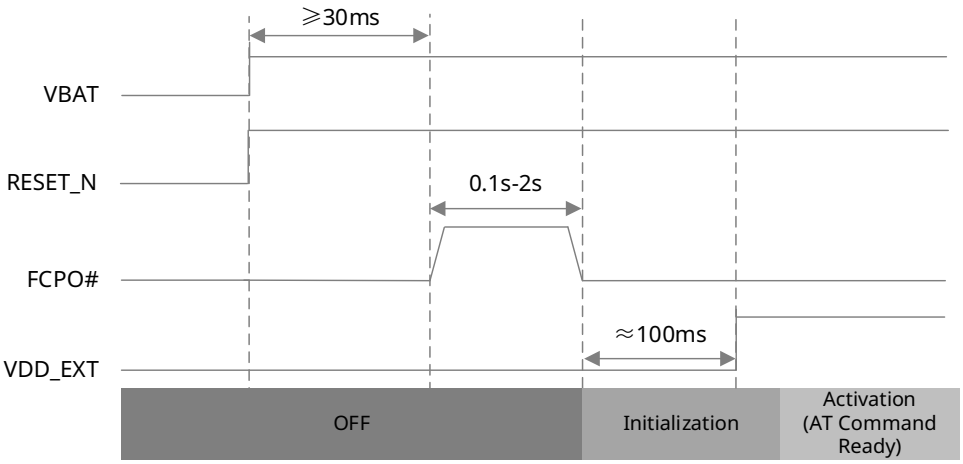

Figure 6. Power-on timing sequence

When the module is in the powered-on state, there are two ways to initiate the power-off process. They are as follows:

- Pulling up the FCPO# pin for 3s to 8s and then releasing it will initiate the power-off process of the module. After releasing the FCPO# signal, there should be a minimum interval of TBD seconds before triggering the next power-on process. This time period is reserved for the module's power-off process.
- By sending the AT+CPWROFF command, you can initiate the soft power-off process of the module.

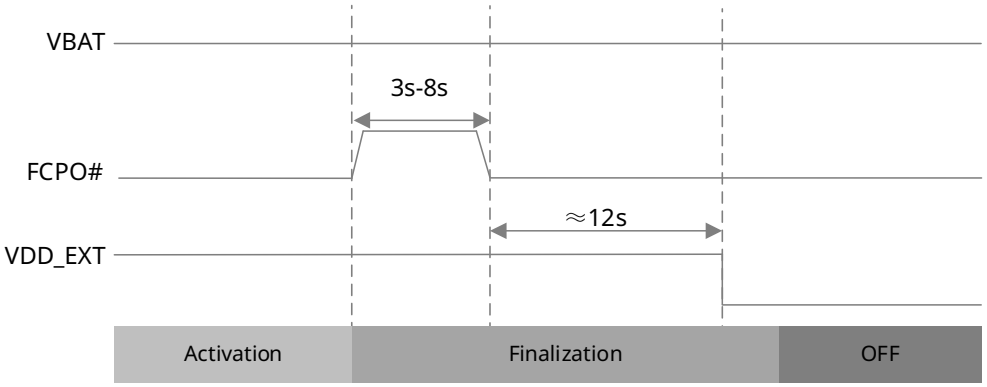

Figure 7. Power-off timing sequence

- When the module is working properly, do not cut off the power supply of the module immediately to avoid damaging the internal flash. It is recommended to start the power-off process with AT command before disconnecting the power supply.
- Ensure VBAT voltage is stable before pulling high FCPO# for power on. It is recommended to pull down FCPO# at least 30ms after VBAT is powered on and stable.
- When using AT command to power off the module, ensure FCPO# is always in low level after the power-off command is executed, otherwise the module will be automatically powered on again after power-off.

4.3 Reset Interface

The module defines two reset modes: hardware reset and software reset. Choose flexibly according to your needs.

Table 6. Reset methods

Reset Mode	Reset Method
Hardware reset	Pulling down the RESET pin for 700ms to 1s and then releasing it will initiate the reset process of the module.
Software reset	Sending the AT command AT+CFUN=15 will initiate the reset process of the module.

The RESET# pin of the module is set to high level by default after module initialization, so no external pull-up is required. When the RESET# pin active low, the module is restarted. It is recommended to add a test point if not use. Reset signal is sensitive to interference, so it is recommended that module interface trace should be as short as possible, and it should be wrapped with ground. Can be controlled using an OC or OD drive circuit or button. The circuit diagram is as follows:

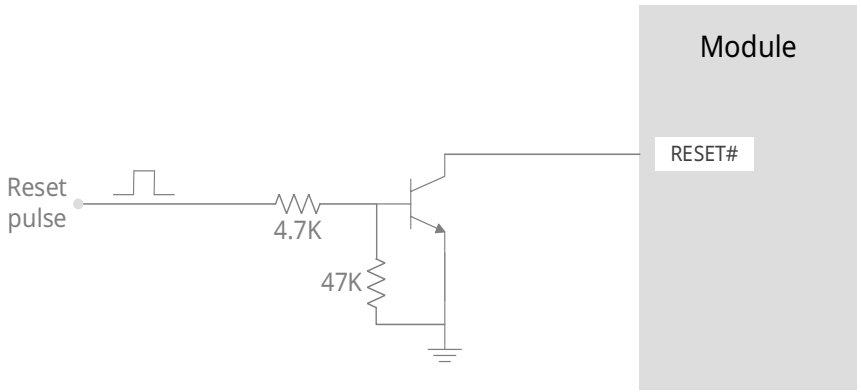

Figure 8. OC drive Reset circuit

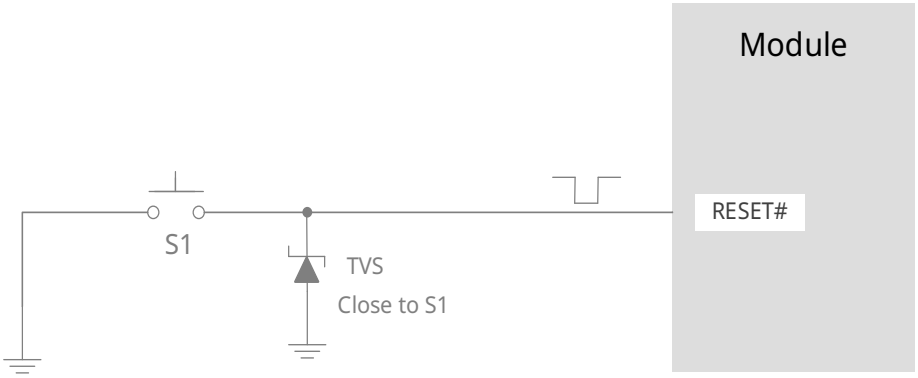

Figure 9. Reset push-button circuit

- It is recommended to execute AT command to restart or operate FCPO# to shutdown first, and use RESET# only after a failed restart or shutdown.
- Ensure that RESET# do not have large load capacitance.

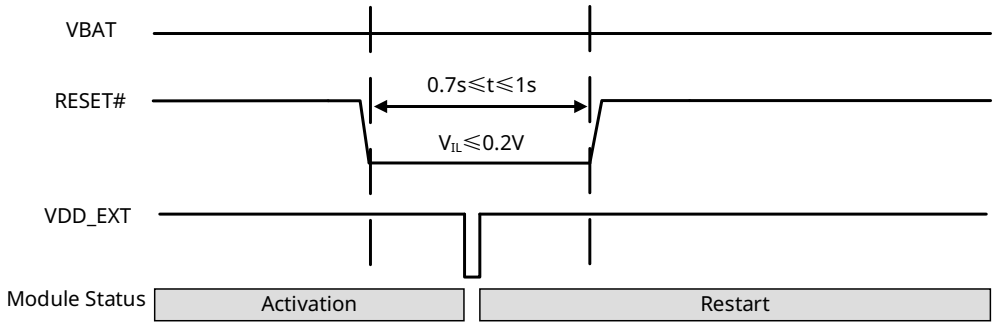

Figure 10. Reset timing sequence

4.4 Forced download

M.2 test points are reserved in the upper left corner of the front, which are the USB-BOOT and VDD_EXT signals of the module, for upgrading the module firmware. Before powering on the module, keep the two points short. After powering on, you can enter the forced download mode, as shown in the following figure.

Figure 11. forced download test points

4.5 PCIe Interface

The module supports one PCIe 2.0 interface that is downward compatible with PCIe 1.0 interface. Support RC and EP mode.

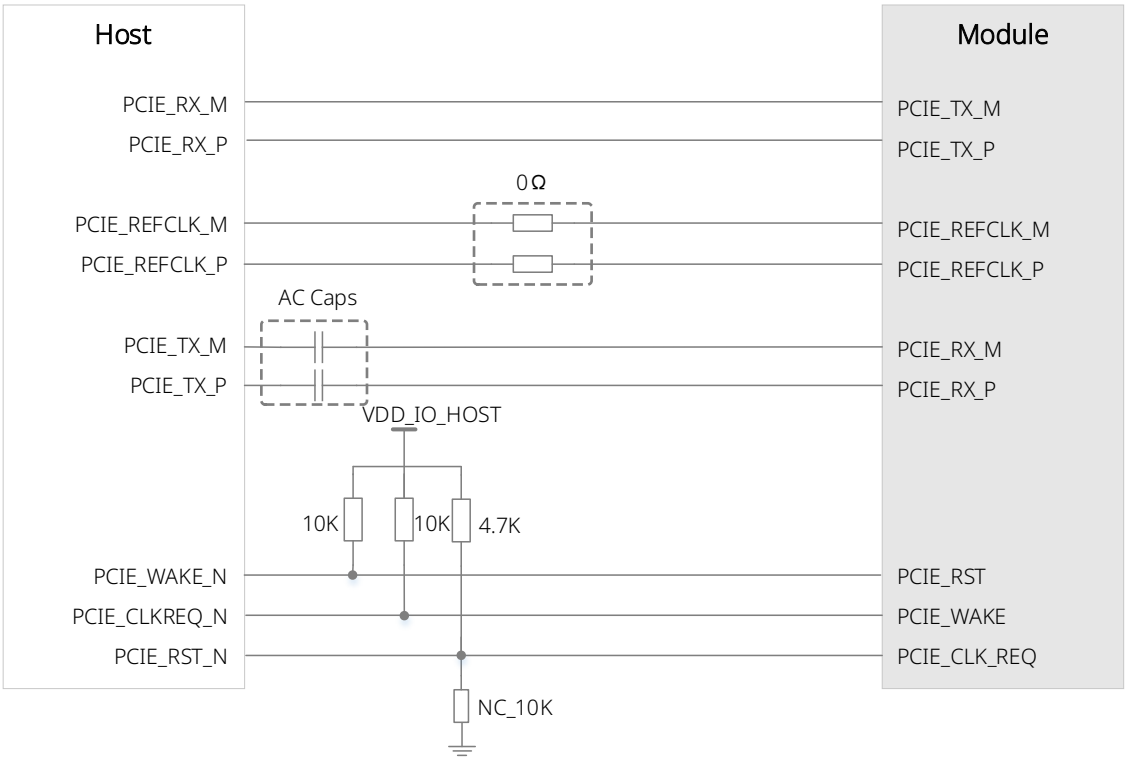

Figure 12. PCIe application circuit

The PCIe 2.0 includes three differential pairs: transmitting pair TXP/N, receiving pair RXP/N and clock pair CLKP/N.

The maximum transmission rate of PCIe reaches 5 GT/s. The rules below must be strictly followed in PCB Layout:

- The differential signal pairs are required to be parallel wires with equal length, and the difference in length is less than 0.7 mm.
- The differential signal pair routes should be as short as possible and be controlled within 200mm for AP end.

- The impedance of differential signal pair routes is recommended to be 85Ω.
- Avoid discontinuous reference ground, such as segment and space.
- When the differential signal routes go through different layers, the via hole of grounding signal should be close to that of signal, and generally, each pair of signals require 1-3 grounding signal via holes and the routes should never cross the segment of plane.
- Try to avoid bended routes and avoid introducing common-mode noise in the system, which will influence the signal integrity and EMI of difference pairs. As shown in the following figure, the bending angle of all routes should be equal to or greater than 135°, the spacing between difference pair routes should be larger than 20 mil, and the routes caused by bending should be greater than 1.5 times route width at least. When a serpentine route is used for length match with another route, the bended length of each segment should be at least 3 times the route width (≥ 3 W). The largest spacing between the bended part of the serpentine route and another one of the differential routes must be less than 2 times the spacing of normal differential routes (S1 < 2S).

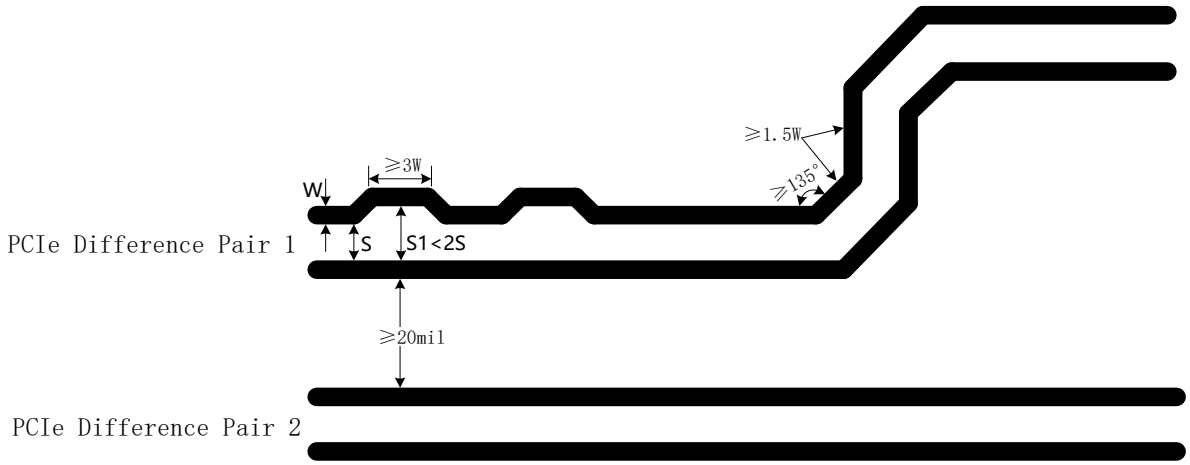

Figure 13. PCIe wiring requirements

- The length match must be met for all parts. When the length match is conducted for the differential lines, the designed position of correct match should be close to that of incorrect match, as shown in the following figure. However, there is no specific requirements for the length match of transmitting pair and receiving pair. That is, the length match is only required in the internal differential lines rather than between different differential pairs. The length match should be close to the signal pin and achieve length match through the small-angle bending design.

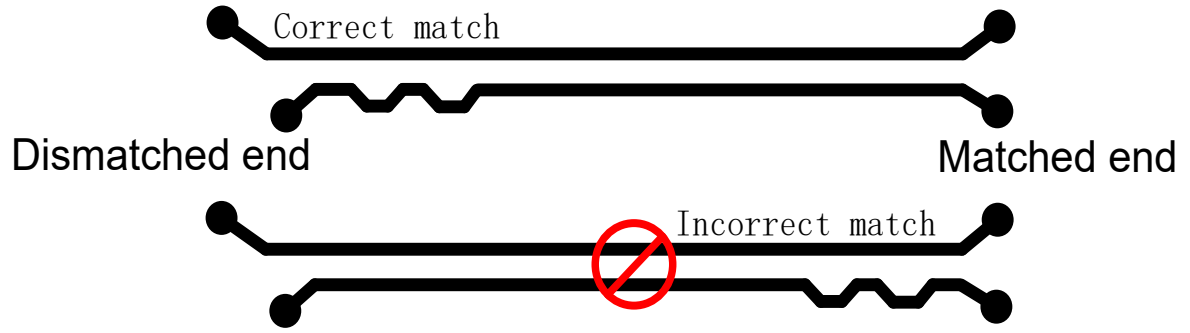

Figure 14. Length match design of differential pairs

4.6 USB Interface

The module provides a USB interface, conforms to the USB 2.0 specification, supports high-speed mode, up to 480Mbps, and is backward compatible with 12Mbps full-speed mode. USB interface supports master and slave mode, which can be used for AT command communication, data transmission, software debugging, firmware upgrade, etc.

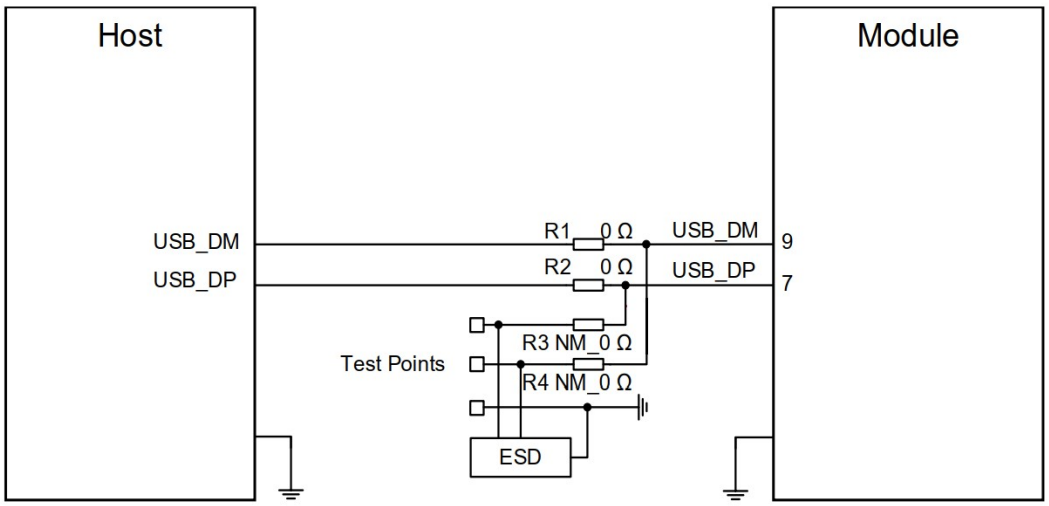

Figure 15. USB 2.0 reference design

It is recommended to series 0R resistor (co-pad with common-mode inductor) between host and module, In order to meet the signal integrity requirements of USB data lines, the common mode inductor should be placed close to the module, traces connecting test points should be kept as short as possible.

The USB 2.0 of the module includes both USB High-Speed (480Mbps) and USB Full-Speed (12Mbps) modes. The equivalent capacitance of the TVS diode on the differential signal lines should be less than 2pF. If there is no ESD risk for the USB interface, the TVS diode can be omitted.

Here are the layout design rules for USB 2.0:

- The differential impedance of USB_D- and USB_D+ signal lines should be controlled within 90Ω±10Ω.
- The length difference between the USB_D- and USB_D+ signal lines should be less than 2 mm, and they should be run in parallel. Avoid routing at right angles.
- It is recommended to route the USB_D- and USB_D+ signal lines on inner layers, with ground planes surrounding on the top, bottom, left and right sides of them for protection.

When not using the USB interface, it is recommended to use the USB 2.0 interface for firmware upgrades and reserve test points for debugging.

4.7 USIM Interface

The module has built-in USIM1 and USIM2 card interfaces, conforms to ETSI and IMT-2000 specifications, supports 1.8V or 3.0V (U)SIM cards, and supports dual card single standby function. The module identifies USIM1 by default and can be switched to USIM2 by the following AT command:

AT+GTDUALSIM=1. For more information, refer to *Fibocom_FG132_AT Commands User Manual.*

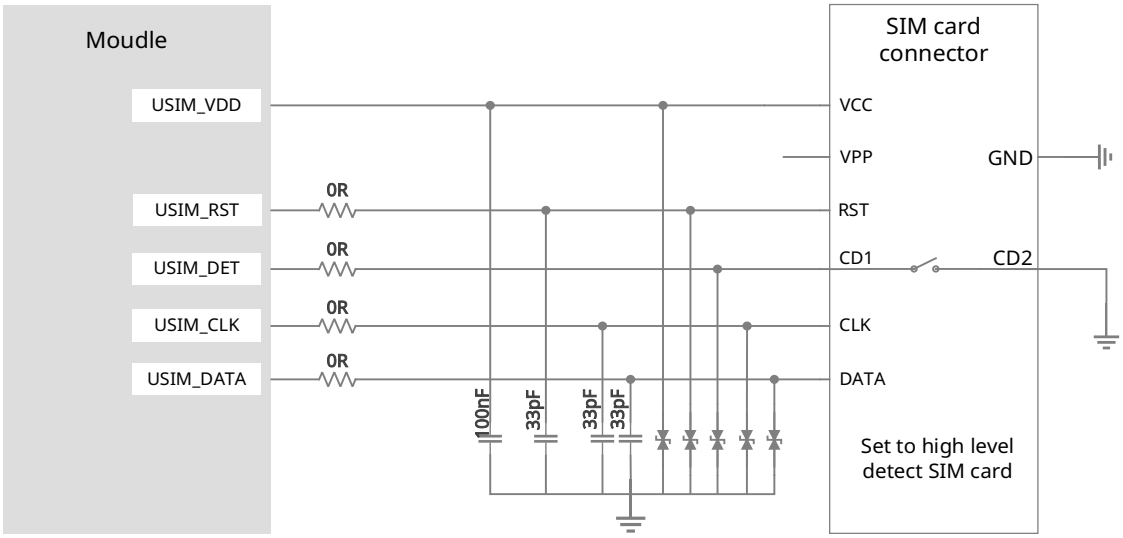

Figure 16. 8 pin SIM card reference circuit

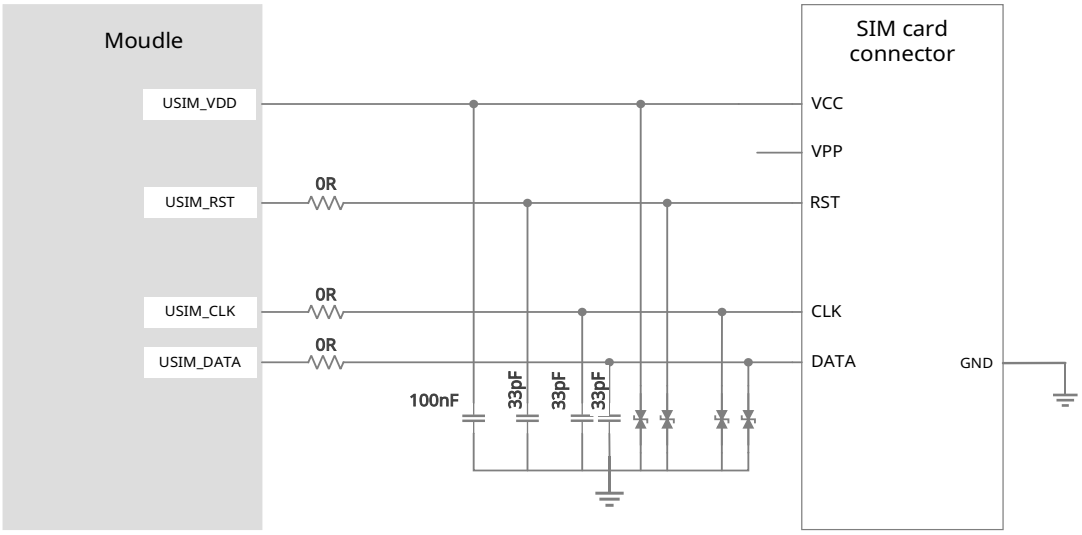

Figure 17. 6 pin SIM card reference circuit

The ESDBL5V0A1 model is recommended for TVS tubes in the above two SIM card reference designs. To ensure the stable operation of USIM cards, the following rules should be strictly followed in the design:

- Place the (U)SIM card slot close to the module and try to ensure that the length of the (U)SIM card

signal trace does not exceed 200 mm.

- It is recommended to route (U)SIM card signal lines in the inner layer with a three-dimensional ground wrapped. It need to be kept away from power lines, crystals, magnetic devices, sensitive signals such as RF signals, analog signals, and noise signals generated by clocks and DC-DCs.
- To prevent crosstalk between the USIM_CLK signal and the USIM_DATA signal, the two traces should not be too close to each other, and a ground shield should be added between the two traces.
- (U)SIM card peripherals is placed as close as possible to the (U)SIM card slot. Add ESD protection devices near the card slot, and the parasitic capacitance of the selected TVS tube is not greater than 15pF. At the same time, a 0 Ω resistor is connected in series between the module and the (U)SIM card slot for debugging. A 33pF capacitor is connected in parallel to the USIM_DATA, USIM_CLK, and USIM_RST signal lines to filter out RF interference.

The module implements hot plug function for the USIM card through the USIM_DET pin. A default high level represents that the SIM card is inserted, while a low level represents that the SIM card is removed. If the user does not need the hot plug function, float USIM_DET. In addition, the hot plug function of USIM card can be enabled and disabled by AT command.

Table 7. Hot plug function of USIM card

AT Command	Function Description	Note
AT+MSMPD=1	Enable the hot plug function detection of USIM card.	- -
AT+MSMPD=0	Disable the USIM card hot plug detection function.	- -

SIM1 hot plug is enabled and SIM2 hot plug is disabled by default. The AT+MSMPD/AT+SIMSWAPCFG command takes effect based on the GTDUALSIM parameter, for example: AT+GTDUALSIM=0, MSMPD and SIMSWAPCFG set hot plug and high/low level detection for SIM1, AT+GTDUALSIM=1, MSMPD and SIMSWAPCFG set hot plug and high/low level detection for SIM2.

4.8 PCM Interface

The module provides a PCM interface and an I2C interface. The PCM interface supports the following two modes:

- Short Frame Mode: The module can be slave or master device.
- Long frame mode: The module can only be a master device.

The module supports 16-bit linear encoding formats. The following timing diagrams are for short frame mode (PCM_SYNC=8kHz, PCM_CLK=2048kHz) and long frame mode (PCM_SYNC=8kHz, PCM_CLK=256kHz).

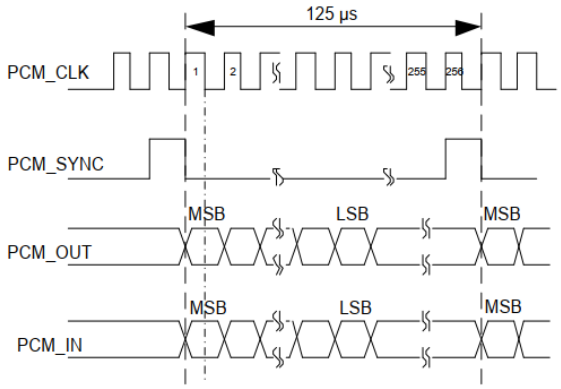

Figure 18. Timing diagram for short frame mode

In short frame mode, data is sampled on the falling edge of PCM_CLK and sent on the rising edge. The falling edge of PCM_SYNC represents a high valid bit. When PCM_SYNC reaches 8kHz, PCM_CLK supports 256kHz, 512kHz, 1024kHz and 2048kHz; when PCM_SYNC reaches 16kHz, PCM_CLK supports 4096kHz.

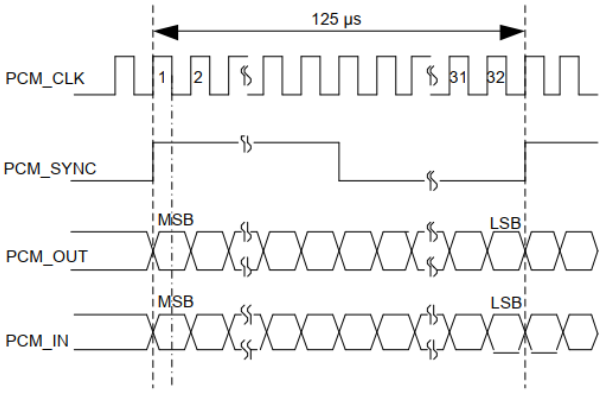

Figure 19. Timing diagram for short frame mode

In long frame mode, data is also sampled on the falling edge of PCM_CLK and sent on the rising edge. The rising edge of PCM_SYNC represents the high valid bit. When PCM_SYNC reaches 8kHz and the duty cycle is 50%, PCM_CLK supports 256kHz, 512kHz, 1024kHz, and 2048kHz.

- It is recommended that RC (R=22Ω, C=22pF) circuits be reserved on the signal lines of the PCM (especially PCM_CLK).
- The module can only be used as a master device in both PCM interface applications and I2C interface applications.

4.9 Network State Indicator Interface

The following figure shows the LED driver circuit.

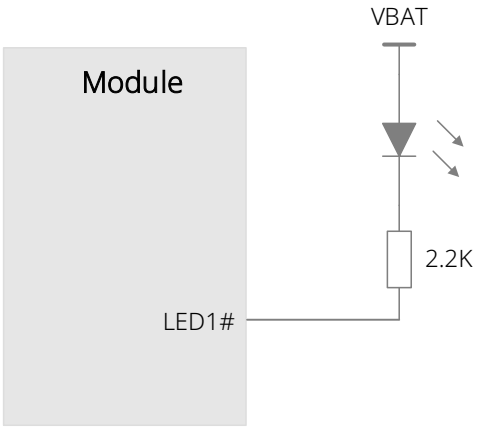

Figure 20. Reference circuit for the network status indicator

The following table describes the working status of the LED1# signal.

Table 8. Working status of the LED1# signal

Pin Name	Module Operating Mode	LED1# signal
LED1#	RF function ON	Low level (LED On)
	RF function OFF	High level (LED Off)

4.10 Flight Mode Control Interface

The module supports two flight mode control methods:

- AT command control method:

  The software defaults to this control method. When the AT+CFUN=4 command is sent, the module enters the flight mode. When the AT+CFUN=1 command is sent, the module enters the operating mode.

- Hardware control method:

  This function is disabled by default. It can be enabled by sending the AT+GTFMODE=1 command through USB. There is a pull-up resistor inside the W_DISABLE1# module by default. When the pin of W_DISABLE1# is pulled up, the module enters the operating mode. When the pin of W_DISABLE1# is pulled down, the module enters the flight mode. This function can be disabled by using the AT+GTFMODE=0 command.

4.11 Host Wakeup Interface

Host can wake up or sleep through the WAKEUP-IN pin control module. When there is a call or text message, the module will pull down the WAKEUP-OUT pin to wake up the host.

The wake-up method and effective power consumption of the module can be configured through AT commands. For detailed instructions, please refer to the sleep wake-up function documentation of relevant products: *Fibocom_MTC_Sleep and Wakeup Application Guide*

4.12 M.2 Interface Type

The M.2 module adopts a 75-pin edge connector as an external interface, where 67 pins are used as signal pins and 8 pins are notch pins. Based on the M.2 interface definition, the module adopts Type 3042-B interface (30 mm × 42 mm, maximum component thickness on the top is 2.4mm, PCB thickness is 0.8 mm, and KEY ID is B).

The following table describes the M.2 interface types.

Table 9. M.2 interface types

Pin	Pin Name	I/O	Reset Value	Pin Description	M.2 Interface Type
1	CONFIG_3	O	- -	NC	WWAN–PCIe Gen2, USB2.0, Defined by Fibocom
21	CONFIG_0	O	- -	NC	
69	CONFIG_1	O	PD	GND	
75	CONFIG_2	O	- -	NC	

5 Antenna Interface

5.1 Antenna Interface Definition

The following table contains all the frequency bands of the series. Please read the definition of the antenna interface carefully and choose the correct antenna interface to connect. If you need other help, contact the Fibocom FAE.

Table 10. Definition of antenna interfaces

Connector	Function Description	TX	RX	Frequency Range
MAIN ANT	TRX	LTE: B1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/30/B34/38/39/40/41/42/43/48/66/71 NR: n1/2/3/5/7/8/12/13/14/18/20/25/26/28/30/38/40/41/48/66/70/71/77/78	LTE: B1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/30/B34/38/39/40/41/42/43/48/66/71 NR: n1/2/3/5/7/8/12/13/14/18/20/25/26/28/30/38/40/41/48/66/70/71/77/78	617MHz~5GHz
DIV ANT	DRX	- -	LTE: B1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/30/B34/38/39/40/41/42/43/48/66/71 NR: n1/2/3/5/7/8/12/13/14/18/20/25/26/28/30/38/40/41/48/66/70/71/77/78	617MHz~5GHz
GNSS ANT	GNSS	- -	GPS/GLONASS/BDS/Galileo/QZSS	1166MHz~1606MHz

5.2 Operating Bands

Table 11. Cellular frequency reference table

Mode	Band	TX (MHz)	RX (MHz)
5G NR	n1	1920~1980	2110~2170
	n2	1850~1910	1930~1990
	n3	1710~1785	1805~1880

Mode	Band	TX (MHz)	RX (MHz)
	n5	824~849	869~894
	n7	2500~2570	2620~2690
	n8	880~915	925~960
	n12	699~716	729~746
	n13	777~787	746~756
	n14	788~798	758~768
	n18	815~830	860~875
	n20	832~862	791~821
	n25	1850~1915	1930~1995
	n26	814~849	859~894
	n28	703~748	758~803
	n30	2305~2315	2350~2360
	n66	1710~1780	2110~2180
	n70	1695~1710	1995~2010
	n71	663~698	617~652
	n38	2570~2620	2570~2620
	n40	2300~2400	2300~2400
	n41	2496~2690	2496~2690
	n48	3550~3700	3550~3700
	n77	3300~4200	3300~4200
	n78	3300~3800	3300~3800
LTE FDD	Band 1	1920~1980	2110~2170
	Band 2	1850~1910	1930~1990
	Band 3	1710~1785	1805~1880
	Band 4	1710~1755	2110~2155
	Band 5	824~849	869~894

Mode	Band	TX (MHz)	RX (MHz)
	Band 7	2500~2570	2620~2690
	Band 8	880~915	925~960
	Band 12	699~716	729~746
	Band 13	777~787	746~756
	Band 14	788~798	758~768
	Band 17	704~716	734~746
	Band 18	815~830	860~875
	Band 19	830~845	875~890
	Band 20	832~862	791~821
	Band 25	1850~1915	1930~1995
	Band 26	814~849	859~894
	Band 28	703~748	758~803
	Band 30	2305~2315	2350~2360
	Band 66	1710~1780	2110~2180
	Band 71	663~698	617~652
LTE TDD	Band 34	2010~2025	2010~2025
	Band 38	2570~2620	2570~2620
	Band 39	1880~1920	1880~1920
	Band 40	2300~2400	2300~2400
	Band 41	2496~2690	2496~2690
	Band 42	3400~3600	3400~3600
	Band 43	3600~3800	3600~3800
	Band 48	3550~3700	3550~3700

5.3 Antenna Performance Requirements

Input impedance: 50 Ω

Input power: >28 dBm

VSWR: <2:1

Antenna gain: <3.6 dBi

Antenna Isolation: >25 dB

Antenna cable insertion loss: LB (<1 GHz)<0.3 dB, MB (1–2.7 GHz)<0.8 dB, HB (>2.7 GHz)<1.2 dB

5.4 RF Connector

Table 12. RF connector performance requirements

Frequency Range	DC to 6 GHz
Characteristic Impedance	50 Ω
Temperature range	-40°C to +85°C

In order to facilitate antenna connection, the module is equipped with a RF connector with the model of ECT 818004607. The size is 2.0 mm × 2.0 mm × 0.6 mm. The following figure shows the connector dimensions.

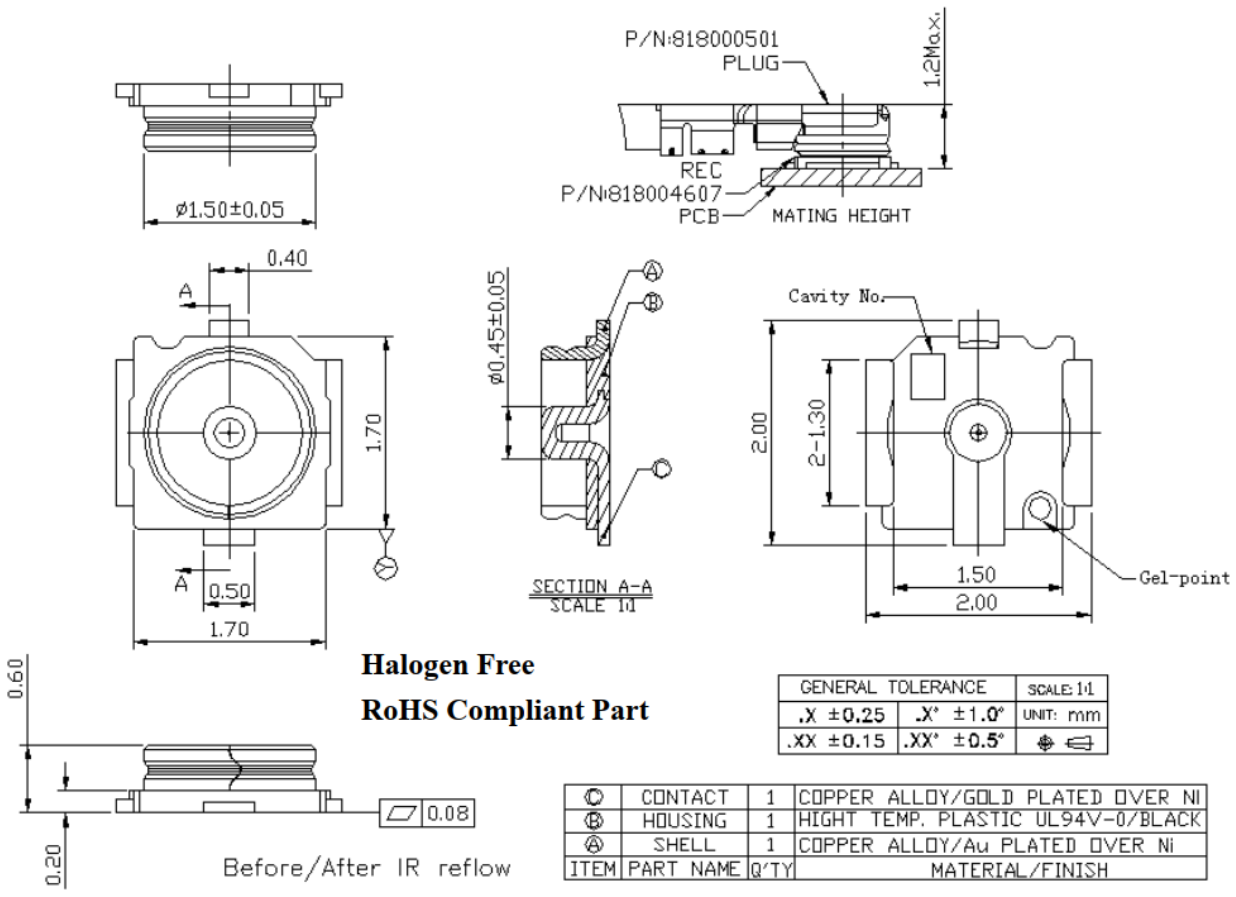

Figure 21. RF connector dimensions

6 Electrical Characteristics

6.1 Logic Level

Table 13. Logic level

Description	Level	Min.	Typical	Max.	Unit
1.8 V logic Level	Digital High level input	1.26	1.8	2.1	V
	Digital Low level input	-0.3	0	0.54	V
	Digital High level output	1.35	1.8	1.8	V
	Digital Low level output	0	0	0.45	V

6.2 Power Consumption

The power consumption measurement is closely related to the operating status of the module. The test conditions are as follows:

The ambient temperature is 25°C, and the power supply voltage is 3.8 V. The USB interface of the module defaults to the Device mode.

Table 14. Power consumption

Parameter	Mode	Condition	Current (mA)
I_{off}	Power off	Power supply Module power-off	0.078
I_{sleep}	Radio off	AT+CFUN=0 AT+GTLPMMODE=1	1.8
	NR FDD	Paging cycle #64 frames (USB Disconnect)	2.7
		Paging cycle #64 frames (USB Suspend)	3.7
		Paging cycle #128 frames (USB Disconnect)	2.4
		Paging cycle #128 frames (USB Suspend)	3.4
		Paging cycle #256 frames (USB Disconnect)	2.2
		Paging cycle #256 frames (USB Suspend)	3.2
		EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Disconnect)	1.9
		EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Suspend)	2.9
		EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Disconnect)	1.8
		EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Suspend)	2.8

		EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Disconnect)	1.8
		EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Suspend)	2.8
		EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Disconnect)	1.8
		EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Suspend)	2.8
	NR TDD	Paging cycle #64 frames (USB Disconnect)	2.7
		Paging cycle #64 frames (USB Suspend)	3.7
		Paging cycle #128 frames (USB Disconnect)	2.4
		Paging cycle #128 frames (USB Suspend)	3.4
		Paging cycle #256 frames (USB Disconnect)	2.2
		Paging cycle #256 frames (USB Suspend)	3.2
		EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Disconnect)	1.9
		EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Suspend)	2.9
		EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Disconnect)	1.8
		EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Suspend)	2.9
		EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Disconnect)	1.8
		EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Suspend)	2.8
		EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Disconnect)	1.8
		EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Suspend)	2.8
	LTE FDD	Paging cycle #64 frames (USB Disconnect)	2.6
		Paging cycle #64 frames (USB Suspend)	3.7
		Paging cycle #128 frames (USB Disconnect)	2.4
		Paging cycle #128 frames (USB Suspend)	3.5
		Paging cycle #256 frames (USB Disconnect)	2.3
		Paging cycle #256 frames (USB Suspend)	3.3
		EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Disconnect)	2
		EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Suspend)	3
		EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Disconnect)	2
		EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Suspend)	3
		EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Disconnect)	2
		EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Suspend)	3
		EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Disconnect)	2
		EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Suspend)	3

	LTE TDD	Paging cycle #64 frames (USB Disconnect)	2.6
		Paging cycle #64 frames (USB Suspend)	3.7
		Paging cycle #128 frames (USB Disconnect)	2.4
		Paging cycle #128 frames (USB Suspend)	3.5
		Paging cycle #256 frames (USB Disconnect)	2.3
		Paging cycle #256 frames (USB Suspend)	3.3
		EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Disconnect)	2
		EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Suspend)	3
		EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Disconnect)	2
		EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Suspend)	3
		EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Disconnect)	2
		EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Suspend)	3
		EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Disconnect)	2
		EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Suspend)	3
I_{IDLE}	NR FDD	Paging cycle #64 frames (USB Disconnect)	10.5
		Paging cycle #64 frames (USB Connect)	19.5
		EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Disconnect)	9
		EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Connect)	18
	NR TDD	Paging cycle #64 frames (USB Disconnect)	10.5
		Paging cycle #64 frames (USB Connect)	19.5
		EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Disconnect)	9
		EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Connect)	18
	LTE FDD	Paging cycle #64 frames (USB Disconnect)	10.5
		Paging cycle #64 frames (USB Connect)	19.5
		EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Disconnect)	10
		EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Connect)	19
	LTE TDD	Paging cycle #64 frames (USB Disconnect)	10.5
		Paging cycle #64 frames (USB Connect)	20
		EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Disconnect)	10
		EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Connect)	19
I_{ACTIVE}	NR FDD	NR FDD Data transfer n1 @+23dBm	610
		NR FDD Data transfer n2 @+23dBm	610

		NR FDD Data transfer n3 @+23dBm	720
		NR FDD Data transfer n5 @+23dBm	650
		NR FDD Data transfer n7 @+23dBm	770
		NR FDD Data transfer n8 @+23dBm	600
		NR FDD Data transfer n12 @+23dBm	600
		NR FDD Data transfer n13 @+23dBm	600
		NR FDD Data transfer n14 @+23dBm	560
		NR FDD Data transfer n18 @+23dBm	620
		NR FDD Data transfer n20 @+23dBm	650
		NR FDD Data transfer n25 @+23dBm	650
		NR FDD Data transfer n26 @+23dBm	610
		NR FDD Data transfer n28 @+23dBm	610
		NR FDD Data transfer n30 @+23dBm	780
		NR FDD Data transfer n66 @+23dBm	650
		NR FDD Data transfer n70 @+23dBm	650
		NR FDD Data transfer n71 @+23dBm	600
	NR TDD	NR TDD Data transfer n38 @+23dBm	250
		NR TDD Data transfer n40 @+23dBm	250
		NR TDD Data transfer n41 @+23dBm	250
		NR TDD Data transfer n48 @+23dBm	250
		NR TDD Data transfer n77 @+23dBm	250
		NR TDD Data transfer n78 @+23dBm	250
	LTE FDD	LTE FDD Data transfer Band 1 @+23dBm	650
		LTE FDD Data transfer Band 2 @+23dBm	650
		LTE FDD Data transfer Band 3 @+23dBm	720
		LTE FDD Data transfer Band 4 @+23dBm	650
		LTE FDD Data transfer Band 5 @+23dBm	650
		LTE FDD Data transfer Band 7 @+23dBm	770
		LTE FDD Data transfer Band 8 @+23dBm	600
		LTE FDD Data transfer Band 12 @+23dBm	650
		LTE FDD Data transfer Band 13 @+23dBm	650
		LTE FDD Data transfer Band 14 @+23dBm	550

		LTE FDD Data transfer Band 17 @+23dBm	650
		LTE FDD Data transfer Band 18 @+23dBm	600
		LTE FDD Data transfer Band 19 @+23dBm	600
		LTE FDD Data transfer Band 20 @+23dBm	650
		LTE FDD Data transfer Band 25 @+23dBm	650
		LTE FDD Data transfer Band 26 @+23dBm	650
		LTE FDD Data transfer Band 28 @+23dBm	600
		LTE FDD Data transfer Band 30 @+23dBm	750
		LTE FDD Data transfer Band 66 @+23dBm	650
		LTE FDD Data transfer Band 71 @+23dBm	600
	LTE TDD	LTE TDD Data transfer Band 34 @+23dBm	350
		LTE TDD Data transfer Band 38 @+26dBm	600
		LTE TDD Data transfer Band 39 @+23dBm	300
		LTE TDD Data transfer Band 40 @+26dBm	650
		LTE TDD Data transfer Band 41 @+26dBm	600
		LTE TDD Data transfer Band 42 @+26dBm	500
		LTE TDD Data transfer Band 43 @+26dBm	450
		LTE TDD Data transfer Band 48 @+23dBm	350

- The above power consumption data is the average measured value, Due to different test condition and consistency, the data floating range is normal within 10%.
- The USB suspend function is turned off by default, if you need to use it, please contact our FAE to provide adaptation services.

6.3 Maximum Transmit Power

The maximum transmit power refers to the power at the antenna pin of the module at an ambient temperature of 25℃. You should fully consider the insertion loss on the RF path when designing, so as not to affect the TRP indicator due to excessive insertion loss. The following table describes the maximum transmit power of the FG132-M. 2 series module.

Table 15. Maximum transmit power

Mode	Band	TX power (dBm)	Comment
NR FDD	n1	23±2	10MHz Bandwidth, inner full
	n2	23±2	10MHz Bandwidth, inner full

Mode	Band	TX power (dBm)	Comment
	n3	23±2	10MHz Bandwidth, inner full
	n5	23±2	10MHz Bandwidth, inner full
	n7	23±2	10MHz Bandwidth, inner full
	n8	23±2	10MHz Bandwidth, inner full
	n12	23±2	10MHz Bandwidth, inner full
	n13	23±2	10MHz Bandwidth, inner full
	n14	23±2	10MHz Bandwidth, inner full
	n18	23±2	10MHz Bandwidth, inner full
	n20	23±2	10MHz Bandwidth, inner full
	n25	23±2	10MHz Bandwidth, inner full
	n26	23±2	10MHz Bandwidth, inner full
	n28	23±2	10MHz Bandwidth, inner full
	n30	23±2	10MHz Bandwidth, inner full
	n66	23±2	10MHz Bandwidth, inner full
	n70	23±2	10MHz Bandwidth, inner full
	n71	23±2	10MHz Bandwidth, inner full
NR TDD	n38	23±2	20MHz Bandwidth, inner full
	n40	23±2	20MHz Bandwidth, inner full
	n41	23±2	20MHz Bandwidth, inner full
	n48	23±2	20MHz Bandwidth, inner full
	n77	23±2	20MHz Bandwidth, inner full
	n78	23±2	20MHz Bandwidth, inner full
LTE FDD	Band 1	23±2	10MHz Bandwidth, 1 RB
	Band 2	23±2	10MHz Bandwidth, 1 RB
	Band 3	23±2	10MHz Bandwidth, 1 RB
	Band 4	23±2	10MHz Bandwidth, 1 RB

Mode	Band	TX power (dBm)	Comment
	Band 5	23±2	10MHz Bandwidth, 1 RB
	Band 7	23±2	10MHz Bandwidth, 1 RB
	Band 8	23±2	10MHz Bandwidth, 1 RB
	Band 12	23±2	10MHz Bandwidth, 1 RB
	Band 13	23±2	10MHz Bandwidth, 1 RB
	Band 14	23±2	10MHz Bandwidth, 1 RB
	Band 17	23±2	10MHz Bandwidth, 1 RB
	Band 18	23±2	10MHz Bandwidth, 1 RB
	Band 19	23±2	10MHz Bandwidth, 1 RB
	Band 20	23±2	10MHz Bandwidth, 1 RB
	Band 25	23±2	10MHz Bandwidth, 1 RB
	Band 26	23±2	10MHz Bandwidth, 1 RB
	Band 28	23±2	10MHz Bandwidth, 1 RB
	Band 30	23±2	10MHz Bandwidth, 1 RB
	Band 66	23±2	10MHz Bandwidth, 1 RB
	Band 70	23±2	10MHz Bandwidth, 1 RB
	Band 71	23±2	10MHz Bandwidth, 1 RB
LTE TDD	Band 34	23±2	10MHz Bandwidth, 1 RB
	Band 38	26±2	10MHz Bandwidth, 1 RB
	Band 39	23±2	10MHz Bandwidth, 1 RB
	Band 40	26±2	10MHz Bandwidth, 1 RB
	Band 41	26±2	10MHz Bandwidth, 1 RB
	Band 42	26±2	10MHz Bandwidth, 1 RB
	Band 43	26±2	10MHz Bandwidth, 1 RB
	Band 48	23±2	10MHz Bandwidth, 1 RB

6.4 Receiving Sensitivity

The receiving sensitivity refers to the sensitivity at the antenna pin of the module at an ambient temperature of 25℃. You should fully consider the insertion loss on the RF path when designing, so as not to affect the TIS indicator due to excessive insertion loss.

Table 16. Dual-antenna receiving sensitivity (dBm)

Band	Sensitivity PRX	Sensitivity DRX	Sensitivity PRX+DRX	3GPP-Requirement
5G NR n1 (20M)	-95	-95.5	-98.5	-93.8
5G NR n2 (20M)	-95.5	-96	-98.5	-91.8
5G NR n3 (20M)	-95	-96	-98.5	-90.8
5G NR n5 (20M)	-96	-97	-99	-90.8
5G NR n7 (20M)	-95	-96	-98	-91.8
5G NR n8 (20M)	-95	-96.5	-99	-85.5
5G NR n12 (10M)	-98	-98	-101.5	-93.8
5G NR n13 (10M)	-98	-98.5	-101.5	-93.8
5G NR n14 (10M)	-98	-98	-101	-93.8
5G NR n18 (10M)	-98	-99.5	-102	-93.8
5G NR n20 (20M)	-95	-96	-98.5	-89.8
5G NR n25 (20M)	-95.5	-96	-98.5	-90.3
5G NR n26 (20M)	-95	-96.5	-99	-87.6
5G NR n28 (20M)	-96.5	-96.5	-99.5	-90.8
5G NR n30 (10M)	-98	-98.5	-101	-95.8
5G NR n38 (20M)	-96	-95.5	-99	-93.8
5G NR n40 (20M)	-95	-96	-98.5	-93.8
5G NR n41 (20M)	-96	-95	-98.5	-91.8
5G NR n48 (20M)	-96	-96	-99.5	-92.8
5G NR n66 (20M)	-95	-95.5	-98.5	-93.3
5G NR n70 (15M)	-97	-97	-100	-95
5G NR n71 (20M)	-96	-95	-97	-86
5G NR n77 (20M)	-96	-96	-99	-92.3
5G NR n78 (20M)	-96	-95.5	-99	-92.8
LTE Band 1(10M)	-98	-99	-101.5	-96.3
LTE Band 2(10M)	-98.5	-99	-102	-94.3

Band	Sensitivity PRX	Sensitivity DRX	Sensitivity PRX+DRX	3GPP-Requirement
LTE Band 3(10M)	-98	-99	-101.5	-93.3
LTE Band 4(10M)	-98	-98.5	-101.5	-96.3
LTE Band 5(10M)	-98.5	-99.5	-102	-94.3
LTE Band 7(10M)	-98	-98.5	-101.5	-94.3
LTE Band 8(10M)	-98.5	-99.5	-102	-93.3
LTE Band 12(10M)	-98.5	-98.5	-101.5	-93.3
LTE Band 13(10M)	-98.5	-99	-101.5	-93.3
LTE Band 14(10M)	-98.5	-98.5	-101.5	-93.
LTE Band 17(10M)	-98.5	-99	-101.5	-93.3
LTE Band 18(10M)	-98.5	-99.5	-102	-96.3
LTE Band 19(10M)	-98.5	-99.5	-102	-96.3
LTE Band 20(10M)	-98.5	-99.5	-102	-93.3
LTE Band 25(10M)	-98.5	-99	-102	-92.8
LTE Band 26(10M)	-98.5	-99.5	-102	-93.8
LTE Band 28(10M)	-99	-99.5	-102	-94.8
LTE Band 30(10M)	-97.5	-98.5	-101.5	-95.3
LTE Band 34(10M)	-98.5	-98.5	-101.5	-96.3
LTE Band 38(10M)	-99	-98	-100.5	-96.3
LTE Band 39(10M)	-98.5	-98.5	-101	-96.3
LTE Band 40(10M)	-97	-98	-100.5	-96.3
LTE Band 41(10M)	-98.5	-97.5	-101	-94.3
LTE Band 42(10M)	-99.5	-99	-102	-95
LTE Band 43(10M)	-99.5	-99	-102	-95
LTE Band 48(10M)	-99.5	-99	-102	-95
LTE Band 66(10M)	-98.5	-99	-101.5	-95.8
LTE Band 71(10M)	-99.5	-98.5	-102	-93.5

6.5 GNSS

The module supports multiple positioning systems including GPS/Beidou/GLONASS/Galileo/QZSS. The module is embedded with LNA, which can effectively improve the sensitivity of GNSS. Test conditions: Power supply voltage 3.8V, ambient temperature 25℃. Use antennas that meet the requirements of section 5.3.

Table 17. GNSS performance

Parameter	Description (instrument test)	Typical Result	Unit
Sensitivity	Acquisition	-146	dBm
	Tracking	-157	dBm
C/N	-130dBm	38.5	dB-Hz
TTFF	Cold Start @all sky	26.67	s
	A-GPS @all sky	9.49	s
	Warm Start @all sky	21.12	s
	Hot Start @all sky	1	s
Static accuracy	CEP-50 @all sky	1.81	m

Table 18. GNSS band

Mode	Band	Unit
GPS/QZSS	L1: 1575.42	MHz
	L5: 1176.45	MHz
GLONASS	L1: 1602	MHz
Beidou	B1I: 1561.098	MHz
	B1C: 1575.42	MHz
	B2A: 1176.45	MHz
Galileo	E1: 1575.42±2.046	MHz
	E5a: 1176.45±10.23	MHz

6.6 Electrostatic Protection

The FG132-M.2 module is a precise electronic product. If ESD protection measures are not taken, a permanent damage may be caused to the module. ESD protection measures should be taken in various links such as R&D debugging, production and assembly, and testing. Therefore, in addition to ESD protection on the package, customers should refer to the recommended design circuits of each interface as much as possible. The following figure shows the ESD protection levels at an ambient temperature of 25℃ and a humidity of 45%.

Table 19. ESD protection levels

Location	Air Discharge	Contact Discharge
GND	±15 kV	±8 kV
Antenna interface	- -	±8 kV
Other interfaces	±1 kV	±0.5 kV

- The data is tested based on Fibocom development board.
- The ESD performance is strongly related to PCB design. Pay special attention to the protection of control signals.
- When designing the whole machine, the GND of the module and the main GND of the large board should maintain sufficient connectivity to ensure that the ESD is discharged through the shortest path.

6.7 Reliability Test

Fibocom's reliability test is carried out at the industrial level. The following table describes the test results of each project.

Table 20. Reliability test results

Test Item	Test Condition
High temperature aging	85°C, 168H/504H/1008H
High temperature and humidity	85°C, 85%RH, 168H/504H/1008H
Corner test	High and low temperature, high and low humidity, high and low voltage, six groups of combinations, and each combination runs for 24 hours
Temperature shock	90/-45°C, 200C
Random vibration	Frequency range: 200Hz to 2000Hz, PSD=0.04 g2/Hz, one hour for X/Y/Z axis
Monomer drop	1m, 6 sides and 2 wheels
Mechanical collision	Peak acceleration: 180m/s2 Pulse duration: 6ms Number of collisions: 1000
Low temperature boot	-40°C, 30 minutes off/5 minutes idle, 3 days
Condensation test	3 days (3 cycles): • First and second cycles with cold cycle • Third cycle without cold cycle
Temperature cycle	85°C/-40°C; 10°C/min; 10min; 240 cycles
Sinusoidal vibration	Amplitude: 3.0G peak to peak Frequency: 5Hz to 500Hz Sweep frequency: 0.5 Octave/min, linear Each axis: 2H
Salt spray	Neutral salt spray, 48H

6.8 Thermal Design

When using M.2 package modules for thermal design of the whole machine, you can refer to the following main suggestions:

- For the M.2 package module, it is preferable to use the whole machine enclosure for heat dissipation above the shield cover, and use a thermal interface material to connect directly above the module and the middle of the enclosure.
- When selecting the enclosure material, it is preferred to choose the metal enclosure. The aluminum alloy material has a better heat dissipation effect.
- If the enclosure is made of plastic, graphite sheets can be pasted on the inside for temperature uniformity to eliminate local hot spots.
- When the distance between the enclosure and the module is relatively long, heat dissipation can be carried out by adding a heat sink on the module.
- The thermal interface material can be filled between the exposed copper area at the bottom of the M.2 package module and the main board PCB for heat dissipation.
- For more thermal design, see *Fibocom_Module General_Thermal Design Guide*.

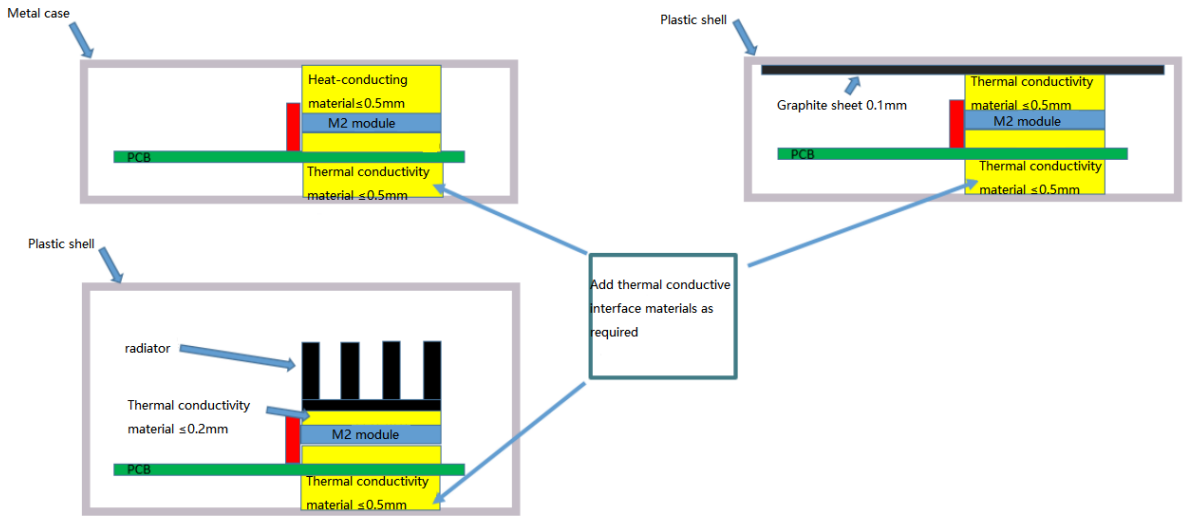

Figure 22. Heat dissipation structure stack

7 Structural Specifications

7.1 Product Appearance

Figure 23. 3042 package product appearance

The pictures are for reference only. Please refer to the actual product for details.

7.2 Structural Dimensions

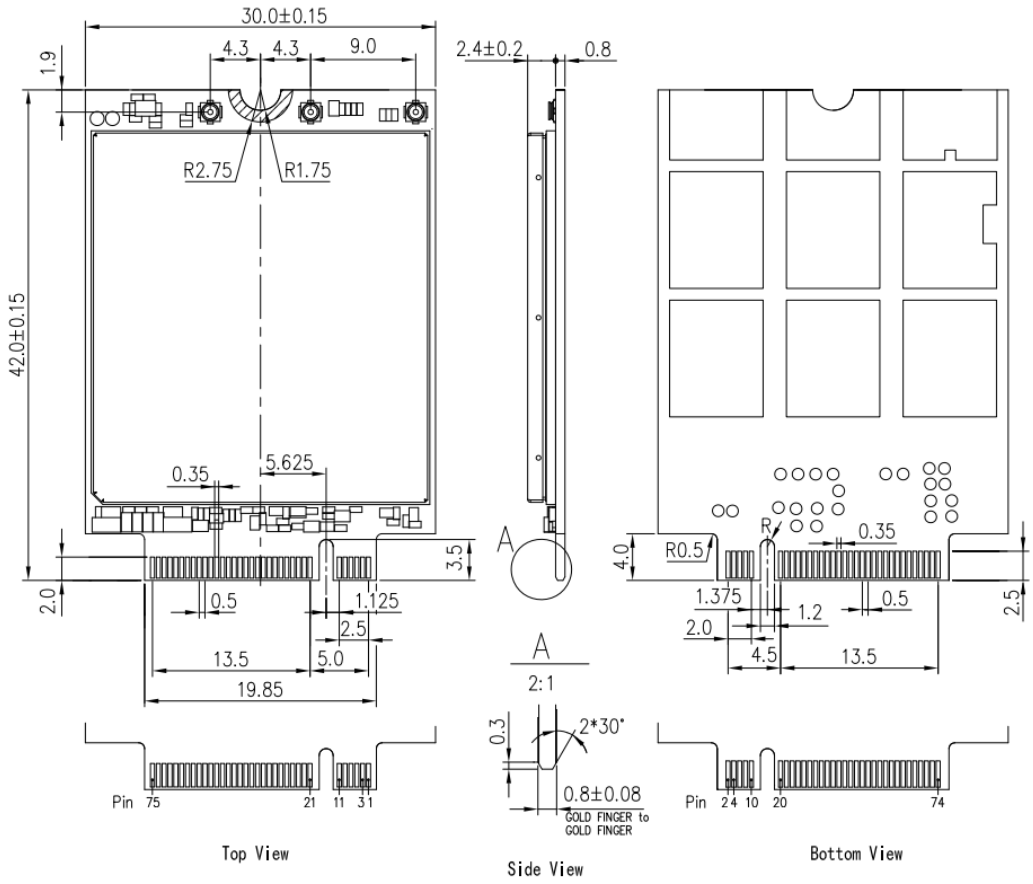

Figure 24. 3042 package structural dimensions (unit: mm)

7.3 M.2 Connector

Connectors that conform to the PCI Express Mini Card standard can be used with this module. It is recommended to choose the LOTES M.2 connector with the model APCI0026-P001A as shown in the following figure. For the package of connector, refer to the specifications.

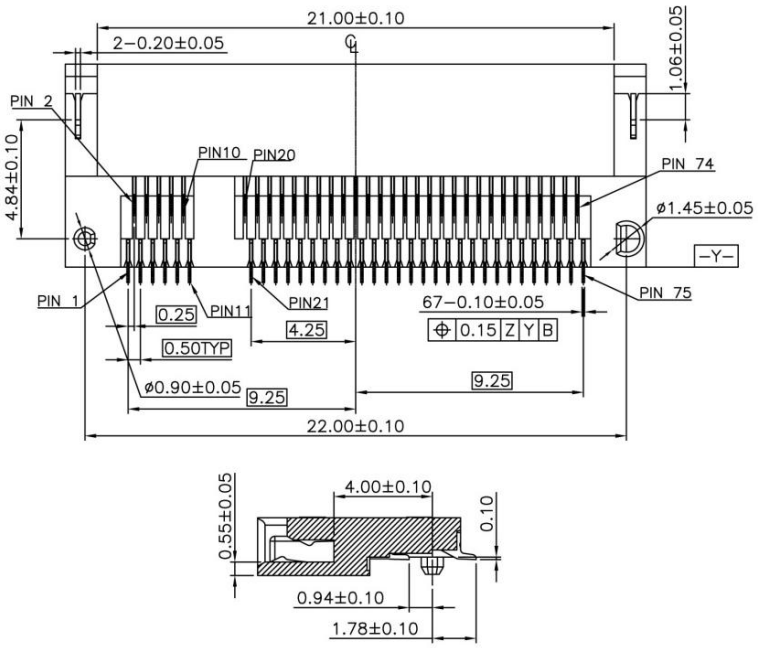

Figure 25. M.2 connector dimensions

8 Storage and Packaging

8.1 Storage Conditions

Modules are shipped in vacuum-sealed bags. module storage should follow the following conditions:

- Storage conditions (recommended): temperature at 23℃±5℃, relative humidity (RH) at 35%–70%.
- Storage period (sealed vacuum packaging): 12 months under the recommended storage conditions.

8.2 Packaging Specifications

The modules are packed in pallets with 20pcs per tray, 5 discs per box (the top layer is an empty tray), 6 boxes per box. Combining the outer packaging mode of hard cartoon boxes, it provides maximum protection for the storage, transportation, and use of modules. the size is shown in the figure below:

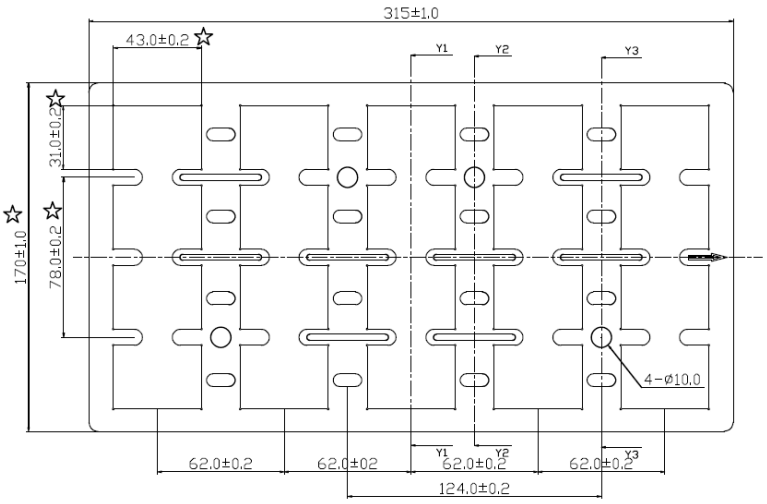

Figure 26. 3042 package tray dimensions (unit: mm)

Appendix A Reference Documents

Fibocom provides the following related documents for your reference. If you have other requirements, please call Fibocom FAE.

Category	Document Name
Software	Fibocom_FG132_AT Commands User Manual
Development suite	Fibocom_EVB-M2-F01_User_Guide
Other	Fibocom_Module General_Thermal Design Guide

Appendix B Acronyms and Abbreviations

Abbreviations	Description
bps	Bits Per Second
CA	Carrier Aggregation
CAT	Category
CPE	Customer Premise Equipment
DRX	Discontinuous Reception
DL	Downlink
DLCA	Downlink Carrier Aggregation
ECC	Envelope Correlation Coefficient
EN-DC	E-UTRA New Radio-Dual Connectivity
FDD	Frequency Division Duplexing
HB	High Band
HSDPA	High Speed Down Link Packet Access
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
Imax	Maximum Load Current
LB	Low Band
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
MB	Middle Band
ME	Mobile Equipment
MIMO	multiple-input and multiple-output
MS	Mobile Station
MT	Mobile Terminated
NR	New Radio
NSA	Non-Standalone
PA	Power Amplifier
PCB	Printed Circuit Board

Abbreviations	Description
PDU	Protocol Data Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
RMS	Root Mean Square
RTC	Real Time Clock
Rx	Receive
SA	Standalone
SCell	Secondary Cell for CA
SMS	Short Message Service
TE	Terminal Equipment
TX	Transmitting
TT	Test Tolerance
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USIM	(Universal) Subscriber Identity Module
VSWR	Voltage Standing Wave Ratio